

# Michael Maniscalco

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## SUMMARY:

Accomplished C++ developer, software architect and CppCon conference speaker, specializing in low latency C++, networking, and lock free algorithms with extensive experience in inventing and engineering high-performance, best in class solutions across various domains in computer science.

## HIGHLIGHTS:

### CppCon Conference Speaker:

- *"Work Contracts: Rethinking Task Based Concurrency and Parallelism for Low Latency C++"*

### FinTech Software Architect/Engineer:

- Linux based development, OS optimizations for low latency
- Architect and sole developer of next gen low latency market data normalization product
- Nanosecond scale, highly deterministic latency
- Distributed architecture - performant and robust
- Designed and implemented ultra performant networking library, efvi, multicast

### Innovations and Algorithms:

- Work Contracts: Ultra low latency, lock free/wait free async task framework - over 100x faster than classic lock free queue based solutions at scale
- Glimpse: Ultra low latency binary logging, instrumentation and visualization for C++
- Data Compression: Invented M03, M99, MSufSort, RLE-EXP

### Academia/Peer Reviewed Publications:

- "An Efficient, Versatile Approach to Suffix Sorting" - ACM JEA v12, Article 1.2
- "Faster Lightweight Suffix Array Construction" - 17th Australasian Workshop on Combinatorial Algorithms

# EXPERIENCE:

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## Lime Trading

*Architect and Principal Developer 2020 - present*

*Director of Engineering - Trade and Execution Services 2017 - 2019*

*Architect and Principal Developer 2015 - 2019*

Highly experienced with optimizing for linux based operating systems, lock free/wait programming, parallelism and concurrency, kernel bypass networking, distributed architecture, interprocess communication, binary protocol processing, market data feeds.

Designed and implemented next generation low latency market data product:

- Replaced existing legacy market data solution, reducing latency by over 50x
- Highly deterministic sub-microsecond low latency performance (*ingress to egress*)
- Distributed, high availability architecture
- Innovative, lock free design based on “work contract” architecture
- Designed highly optimized kernel bypass networking library based on ef\_vi
- Support for NYSE, Nasdaq, OTC, CBOE and OPRA feeds
- Produced normalized non-display market data via multicast for consumers
- Designed consumer libraries for different consumer profiles:
  - Multicast receiver library only
  - Multicast receiver with book building
  - Multicast receiver, book building and lock free multi core API
- Integration with trading engine reduced latencies by several microseconds

Maintained legacy market data solution:

- Update market feed format changes, multicast group changes, minor defect fixes
- Updated code base from gcc 4 to gcc 13, allowing for use of modern C++

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## Hydrolix

*Principal Developer 2019 - 2020*

Principal developer for stealth mode startup, data specific compression algorithms for databases, SIMD.

- Invented M99b, SIMD based integer compression engine designed for compression of integer columns in databases.
- Wrote daemon process used in the collection of performance metrics from the main product which was then streamed off box for analytics.

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## Viasat/Intelligent Compression Technologies

Senior Developer 2002 - 2015

Data Compression, Algorithmic Development, WAN acceleration.

- Wrote all data compression engines
- Patent for delta compression engine
- Video predictive block compression algorithm
- Associative HTTP prefetching - early machine learning architecture for predicting browsing behavior to pre-position content on local machine to reduce latency
- Microsoft Exchange accelerator - reverse engineered protocol to build accelerator over WAN

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## PERSONAL PROJECTS/PORTFOLIO:

### Work Contract Library:

[github.com/buildingcpp/work\\_contract](https://github.com/buildingcpp/work_contract)

Presented at CppCon 2024 - [https://www.youtube.com/watch?v=oj\\_vpZNMVw](https://www.youtube.com/watch?v=oj_vpZNMVw)

A simple, low latency, lock free/wait free threading and asynchronous task management system. Vastly more scalable than lock free MPMC task queues capable of over 100x throughput at scale.

### Asynchronous Networking Library:

[github.com/buildingcpp/network](https://github.com/buildingcpp/network)

A simple, easy to use networking library designed to showcase "Work Contracts". Supports asynchronous send and receive for TCP, UDP and UDP Multicast.

### Messaging Library:

[github.com/buildingcpp/message](https://github.com/buildingcpp/message)

A highly extensible, binary messaging library. Makes defining and processing protocols trivially easy. Designed for ultra low latency with dead simple (almost impossible to make a mistake) message parsing and marshaling.

### Glimpse Instrumentation Library:

[github.com/buildingcpp/glimpse](https://github.com/buildingcpp/glimpse) [private]

Ultra low latency, object oriented, application instrumentation and graphical analysis tools. Incredibly low overhead (less than one nanosecond per entry at scale) streaming instrumentation which can be sampled, visualized and mined by powerful visual tools.

### **Various Novel Data Compression Algorithms:**

[github.com/michaelmaniscalco](https://github.com/michaelmaniscalco)

M99, M03, RLE-EXP compression algorithms, and MSufSort SACA algorithm.

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## **PUBLICATIONS:**

### **An Efficient, Versatile Approach to Suffix Sorting:**

Maniscalco & Puglisi - ACM Journal of Experimental Algorithmics Volume 12, Article 1.2

[www.michael-maniscalco.com/download/10.1.1.184.56.pdf](http://www.michael-maniscalco.com/download/10.1.1.184.56.pdf)

### **Faster Lightweight Suffix Array Construction:**

Maniscalco & Puglisi - 17th Australasian Workshop on Combinatorial Algorithms (AWOCA'06)

[www.michael-maniscalco.com/download/10.1.1.183.9182.pdf](http://www.michael-maniscalco.com/download/10.1.1.183.9182.pdf)

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## **PATENTS:**

### **Methods and systems for utilizing delta coding in acceleration proxy servers**

Patent #US8010705B1

### **Selective Prefetch Scanning**

Patent #US9407717B1